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buried drain line and the deep doped region together form a bit line of the memory device;

forming an insulation layer on the gate oxide layer and above the bit line;

removing the cap layer;

forming a conductive layer on the substrate; and

patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.

## REMARKS

### Present Status of the Application

The Office Action rejected claims 1-3 and 5-17 under 35 U.S.C. 102(b), as being anticipated by Tsutsumi (US Patent No. 6,087,727). Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumi. Claims 1 and 6 have been amended. This Amendment is promptly filed to place the above-captioned case in condition for allowance. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After considering the following remarks, a notice of allowance is respectfully solicited.

### Discussion of 102 and 103 Rejections

*Claims 1-3 and 5-17 stand rejected under 35 U.S.C. 102(b), as being anticipated by Tsutsumi (US Patent No. 6,087,727).*

Applicants respectfully traverse the rejections for at least the reasons set forth below.

The independent claims 1 and 6 have been amended to more clearly define the device and the fabrication method according to the present invention. No new matter has been added to the application by the amendments made to the claims, and the supporting grounds for the amendment can be found at least in Figs. 2E-2G. From Fig. 6, it clearly shows that the insulation layer 218 is disposed on the gate oxide layer 202, between spacers 212 and above the bit line 217. Therefore, in the present invention, the insulation layer is disposed on the gate oxide layer and above the bit line.

As amended, claims 1 and 6 respectively recite:

1. (Once Amended) A memory device, comprising
a substrate;
a gate oxide layer, disposed on a surface of the substrate;
a gate, disposed on a portion of the gate oxide layer;
a buried drain line, located in the substrate beside both sides of the gate;
a spacer, disposed on sidewalls of the gate;
***a deep doped region, located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device***;
***an insulation layer, disposed on the gate oxide layer and above the bit line***; and
a word line, disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

6. (Once Amended) A fabrication method for a memory device, comprising:
forming a gate oxide layer on a substrate;
forming a bar-shaped conductive structure on the gate oxide layer, wherein a cap layer is formed on a top of the bar-shaped conductive structure;
forming a buried drain line in the substrate beside both sides of the bar-shaped conductive structure;
forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer;
***forming a deep doped region in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device***;
***forming an insulation layer on the gate oxide layer and above the bit line***;
removing the cap layer;
forming a conductive layer on the substrate; and
patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.

***(Emphasis added)***

Applicant respectfully asserts that the memory device claimed in the present invention patentably distinguishes over Tsutsumi's device, because the Tsutsumi reference lacks these features emphasized above (in bold). Tsutsumi discloses a semiconductor device including source/drain electrodes 18a/18b connected to n- (12a/12b) and n+ source/drain regions (16a/16b), a gate electrode 11 on a gate insulating film 7 of an MISFET. The source/drain electrodes, acting as a bit line, are insulated by sidewall insulating films 15 and silicon oxide film 19, while a first interconnection 20 connecting to the gate electrode constitutes a word line of the MISFET. However, Tsutsumi emphasize that the source/drain electrodes 18a/18b on the source/drain regions (16a/16b) constitute the bit line. Therefore, the silicon oxide film 19 is located on the sour/drain electrodes 18a/18b (the bit line), but not on or even adjoining to the gate insulating film 7.

The Tsutsumi reference fails to teach or suggest the insulation layer disposed on the gate oxide layer and above the bit line as claimed in the present invention. Moreover, Tsutsumi does not teach or suggest the buried drain line and the deep doped region together form a bit line. Therefore, Tsutsumi did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in independent claims 1 and 6. For at least the foregoing reasons, all pending claims patently define over the cited references and should be allowed. Withdrawal and reconsideration of this 102 rejection are respectfully requested.

*Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tsutsumi.*

Dependent claim 4 is submitted to be patentably distinguishable over the cited reference for at least the same reasons as independent claim 1, from which this claim respectively depends,

as well as for the additional features that this claim recites. Claim 4 is believed allowable and such allowance is respectfully requested.

As a result, withdrawal of this 103 rejection is respectfully requested.

## CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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## MARKED VERSION TO SHOW CHANGE

In The Claim

1. (Once Amended) A memory device, comprising

a substrate;

a gate oxide layer, disposed on a surface of the substrate;

a gate, disposed on a portion of the gate oxide layer;

a buried drain line, located in the substrate beside both sides of the gate;

a spacer, disposed on sidewalls of the gate;

a deep doped region, located in the substrate below a part of the buried drain line, wherein the buried drain line and the deep doped region together form a bit line of the memory device;

an insulation layer, disposed on the gate oxide layer and above the bit line; and

a word line, disposed above the gate and the insulation layer, perpendicular to a direction of the bit line.

6. (Once Amended) A fabrication method for a memory device, comprising:

forming a gate oxide layer on a substrate;

forming a bar-shaped conductive structure on the gate oxide layer, wherein a cap layer is formed on a top of the bar-shaped conductive structure;

forming a buried drain line in the substrate beside both sides of the bar-shaped conductive structure;

forming a spacer on sidewalls of the bar-shaped conductive structure and the cap layer;

forming a deep doped region in the substrate beside both sides of the spacer, wherein the buried drain line and the deep doped region together form a bit line of the memory device;

forming an insulation layer on the gate oxide layer and above the bit line;

removing the cap layer;

forming a conductive layer on the substrate; and

patterning the conductive layer and the bar-shaped conductive structure in a direction perpendicular to a direction of the bit line to form a word line and a plurality of gates.